-- 24. A semiconductor memory comprising:

a plurality of first regions arranged in lattice fashion, each of which corresponds to a memory array including a plurality of main word lines extending in a first direction, a plurality of sets of sub-word lines extending in said first direction, a plurality of pairs of data lines extending in a second direction perpendicular to said first direction and a plurality of memory cells, each of which is coupled to a corresponding one of said plurality of sub-word lines and a corresponding one of said data lines, one of said plurality of main word lines being allotted to one of said plurality of sets of sub-word lines;

a plurality of second regions, each of which is arranged alternately with each of said first regions arranged along said first direction and each of which includes sub-word line drivers connected to said sub-word lines;

a plurality of third regions, each of which is arranged alternately with each of said first regions arranged along said second direction and each of which includes sense amplifiers connected to said data lines; and

a plurality of fourth regions, each of which is arranged alternately with each of said third regions arranged along said first direction,

wherein each of said plurality of main word lines extends through one or more of said first regions arranged along said first direction;

wherein said semiconductor memory further includes:

a plurality of pairs of sub-common data lines, each of which extends through said third regions arranged along said first direction;

Q2 cont'd

first switching circuits formed in said third regions and connected interposingly between said plurality of pairs of data lines and a corresponding one of said pairs of sub-common data lines;

a plurality of pairs of main-common data lines, each of which extends through one or more of second regions arranged along said second direction; and

second switching circuits formed in said fourth regions and connected interposingly between a corresponding one of said pairs of main-common data lines and a corresponding one of said pairs of sub-common data lines.

2.

2~~5~~. A semiconductor memory according to claim 2~~4~~ 1,

wherein a number of memory arrays allotted to one of said main word-lines is greater than a number of memory arrays allotted to a corresponding one of said pairs of sub-common data lines.

3.

2~~6~~. A semiconductor memory according to claim 2~~4~~ 1,

wherein a length of said each main word-line is longer than a length of said each pair of sub-common data lines.

4.

2~~7~~. A semiconductor memory comprising:

a first region extending in a first direction;

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a second region extending in said first direction and in parallel with said first region;

a third region extending in a second direction perpendicular to said first direction;

a fourth region formed as a rectangle, two sides of which are contiguous to said first region and said third region, respectively; and

a fifth region formed as a rectangle, three sides of which are contiguous to said first region, said second region and said third region, respectively;

wherein said third region includes a pair of main common data lines extending in said second direction,

wherein said fourth region includes a first memory array having a plurality of first main word lines extending in said first direction, a plurality of sets of first sub-word lines extending in said first direction, a plurality of pairs of first data lines extending in said second direction and a plurality of first dynamic memory cells, each of which is coupled to a corresponding one of said plurality of first sub-word lines, each of said sets of first sub-word lines corresponding to one of said plurality of first main word lines,

wherein said fifth region includes a second memory array having a plurality of second main word lines extending in said first direction, a plurality of sets of second sub-word lines extending in said first direction, a plurality of pairs of second data lines extending in said second direction and a plurality of second dynamic memory cells, each

of which is coupled to a corresponding one of said plurality of second sub-word lines, each of said sets of second sub-word lines corresponding to one of said plurality of second main word lines,

A2 cont

wherein said first region includes:

(1) a pair of first sub-common data lines extending in said first direction,

(2) first sense amplifiers connected to said plurality of pairs of first data lines and

(3) first switching circuits connected interposingly between said plurality of pairs of first data lines and said pair of first sub-common data lines,

wherein said second region includes:

(1) a pair of second sub-common data lines extending in said first direction,

(2) second sense amplifiers connected to said plurality of pairs of second data lines, and

(3) second switching circuits connected interposingly between said plurality of pairs of second data lines and said pair of second sub-common data lines,

wherein said first region and said third region intersect in a first crossing area including:

(1) a third switching circuit connected interposingly between said pair of main common data lines,

(2) a fourth switching circuit which provides said first sense amplifiers with a first positive power supply voltage, and

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(3) a fifth switching circuit which provides said first sense amplifiers with a second positive power supply voltage lower than said first positive power supply voltage, and

wherein said second region and said third region intersect in a second crossing area including:

A2 cont'd

(1) a sixth switching circuit connected interposingly between said pair of main common data lines,

(2) a seventh switching circuit which provides said second sense amplifiers with said first positive power supply voltage, and

(3) an eighth switching circuit which provides said second sense amplifiers with said second positive power supply voltage.

5. 4
~~2~~. A semiconductor memory according to claim ~~2~~, wherein said third region includes first sub-word line drivers coupled to said first sub-word lines and second sub-word line drivers coupled to said second sub-word lines.

6. 4
~~2~~. A semiconductor memory according to claim ~~2~~, wherein each of said first and second sense amplifiers includes a pair of PMOS transistors and a pair of NMOS transistors, each of said pairs of PMOS and NMOS transistors having sources coupled in common, drains coupled to corresponding pairs of data lines and dates cross-coupled to said drains,

wherein each of said first and second sense amplifiers provides said corresponding pair of data lines with

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a pair of complementary signals having a high side voltage and a low side voltage on the basis of information of a corresponding one of said dynamic memory cells,

wherein, in a first period, said first and second sense amplifiers are driven by said first positive power supply voltage, and

wherein, in a second period following said first period, said first and second sense amplifiers are driven by said second positive power supply voltage.

37. A semiconductor memory comprising:

a first region extending in a first direction;

a second region extending in said first direction and in parallel with said first region;

a third region extending in a second direction perpendicular to said first direction;

a fourth region formed as a rectangle, two sides of which are contiguous to said first region and said third region, respectively; and

a fifth region formed as a rectangle, three sides of which are contiguous to said first region, said second region and said third region, respectively;

wherein said third region includes a pair of main common data lines extending in said second direction,

wherein said fourth region includes a first memory array having a plurality of first main word lines extending in said first direction, a plurality of sets of first sub-word lines extending in said first direction, a plurality of pairs

of first data lines extending in said second direction and a plurality of first dynamic memory cells, each of which is coupled to a corresponding one of said plurality of first sub-word lines, each of said sets of first sub-word lines corresponding to one of said plurality of first main word lines,

A2 cont'd

wherein said fifth region includes a second memory array having a plurality of second main word lines extending in said first direction, a plurality of sets of second sub-word lines extending in said first direction, a plurality of pairs of second data lines extending in said second direction and a plurality of second dynamic memory cells, each of which is coupled to a corresponding one of said plurality of second sub-word lines, each of said sets of second sub-word lines corresponding to one of said plurality of second main word lines,

wherein said first region includes:

(1) a pair of first sub-common data lines extending in said first direction,

(2) first sense amplifiers connected to said plurality of pairs of first data lines and

(3) first switching circuits connected interposingly between said plurality of pairs of first data lines and said pair of first sub-common data lines,

wherein said second region includes:

(1) a pair of second sub-common data lines extending in said first direction,

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(2) second sense amplifiers connected to said plurality of pairs of second data lines, and

(3) second switching circuits connected interposingly between said plurality of pairs of second data lines and said pair of second sub-common data lines,

A2 Contd

wherein said first region and said third region intersect in a first crossing area including a third switching circuit connected interposingly between said pair of first sub-common data lines and said pair of main common data lines,

wherein said second region and said third region intersect in a second crossing area including a fourth switching circuit connected interposingly between said pair of second sub-common data lines and said pair of main common data lines, and

wherein each of said first and second sub-word line drivers include:

(1) a first PMOS transistor having a gate connected to a corresponding one of said main word lines, a drain connected to a corresponding one of said sub-word lines and a source receiving a first signal,

(2) a first NMOS transistor having a gate connected to the gate of said first PMOS transistor, a drain connected to the drain of said first PMOS transistor and a source connected to a ground potential, and

(3) a second NMOS transistor having a drain connected to the drain of said first NMOS transistor, a source connected to said ground potential and a gate receiving a second

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signal, said first and second signals being complementary signals.

8. 31. A semiconductor memory according to claim 30, wherein said semiconductor memory is formed on a P-type substrate comprising:

(1) a first N-well,

(2) a second N-well formed in said first N-well,

(3) a first P-well formed in said first N-well, and

(4) a second P-well formed in said first N-well,

wherein the source and the drain of said first PMOS are in said second N-well,

wherein the source and the drain of said first NMOS are in said first P-well, and

wherein the source and the drain of a switching NMOS transistor, forming one of said dynamic memory cells, are in said second P-well.

9. 32. A semiconductor memory according to claim 31, wherein said first N-well is supplied with a voltage corresponding to a high level of said first signal, and

wherein said P-type substrate is supplied with said ground potential. --

REMARKS

Entry of this amendment prior to examination is respectfully requested.